USBMOD5 - USB Dual Channel UART/FIFO Development Module

The USBMOD5 shown in Diagram 1 is an integrated module based on the FTDI FT2232C Dual Channel USB UART / FIFO IC. The module features two Multi-purpose UART/FIFO controllers that can be configured in several different modes depending on the application.

The module's 40 pin Dual Inline Package (DIP) fits into a standard 40 pin 600mil wide IC Socket. This makes the USBMOD5 ideal for rapid prototyping and development work.

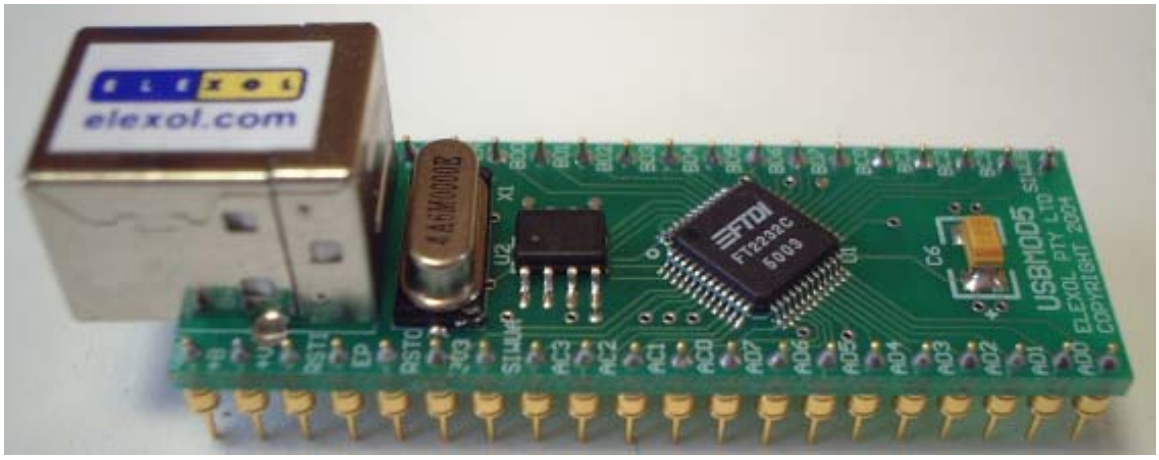


Diagram 1

MODULE FEATURES

- Single module Dual Channel UART/FIFO USB solution
- Based on the FTDI FT2232C Dual Channel USB UART / FIFO IC
- Integrated Type-B USB Connector
- On-board 6MHz Crystal
- External EEPROM on board for USB enumeration data
- No external passive components required
- 40-pin Dual In-Line Package Ideal for prototyping
- Fits into a standard 40-pin 600mil IC Socket

FT2232C IC FEATURES

- Single Chip USB - Dual Channel Serial /Parallel Ports with a variety of configurations
- Entire USB protocol handled on the chip...no USB- specific firmware programming required
- FT232BM-style UART interface option with full Handshaking & Modem interface signals
- UART Interface supports 7/ 8 bit data, 1/ 2 stop bits, and Odd/ Even/ Mark/ Space/ No Parity
- Transfer Data Rate 300 to 1 Mega Baud (RS232)
- Transfer Data Rate 300 to 3 Mega Baud (TTL and RS422 /RS485)
- Auto Transmit Enable control for RS485 serial applications using TXDEN pin

- FT245BM-style FIFO interface option with bi-directional data bus and simple 4-wire handshake interface
- Transfer Data Rate up to 1 Megabyte /Second
- Enhanced Bit-Bang Mode interface option
- New Synchronous Bit-Bang Mode interface option
- New CPU-Style FIFO Interface Mode option
- New Multi-Protocol Synchronous Serial Engine (MPSSE) interface option
- New MCU Host Bus Emulation Mode option
- New Fast Opto-Isolated Serial Interface Mode option
- Interface mode and USB Description strings configurable in external EEPROM
- EEPROM Configurable on board via USB
- Support for USB Suspend and Resume conditions via PWREN#,and SI /WU pins
- Support for bus powered, self powered, and high-power bus powered USB configurations
- Integrated Power-On-Reset circuit, with optional Reset input and Reset Output pins
- 5V and 3.3V logic IO Interfacing with independent level conversion on each channel
- Integrated 3.3V LDO Regulator for USB IO
- Integrated 6MHz – 48Mhz clock multiplier PLL
- USB Bulk or Isochronous data transfer modes
- 4.35V to 5.25V single supply operating voltage range
- UHCI /OHCI /EHCI host controller compatible
- USB 2.0 Full Speed (12 Mbits /Second) compatible
- Compact 48-LD LQFP package

VIRTUAL COM PORT (VCP) DRIVERS for

- Windows 98 /98 SE /2000 /ME /XP
- Windows CE **
- MAC OS-8 and OS-9**
- MAC OS-X**
- Linux 2.40 and greater**

D2XX (USB Direct Drivers +DLL S/W Interface)

- Windows 98 /98 SE /2000 /ME /XP

APPLICATION AREAS

- USB - Dual Port RS232 Converters
- USB - Dual Port RS422 /RS485 Converters
- Upgrading Legacy Peripheral Designs to USB
- USB Instrumentation
- USB JTAG Programming
- USB to SPI Bus Interfaces
- USB Industrial Control
- Field Upgradeable USB Products
- Galvanically Isolated Products with USB Interface

[**=In planning or under development]

ENHANCEMENTS

The FT2232C incorporates all of the enhancements introduced for the second generation FT232BM and FT245BM chips. These are summarised as follows: -.

- **Two Individually Configurable IO Channels**
  Each of the FT2232C 's Channels (A and B) can be individually configured as a FT232BM-style UART interface, or as a FT245BM-style FIFO interface. In addition these channel can be configured in a number of special IO modes.
- **Integrated Power-On-Reset (POR) circuit**
  The device incorporates an internal POR function. A RESET# pin is available to allow external logic to reset the device where required, however for most applications this pin can simply be hardwired to Vcc. A RSTOUT# pin is provided in order to allow the new POR circuit to provide a stable reset to external MCU and other devices.
- **Integrated RCCLK circuit**
  Used to ensure that the oscillator and clock multiplier PLL frequency are stable prior to USB enumeration.

- **Integrated level converter on UART /FIFO interface and control signals**
  Each channel of the FT2232C has its own independent VCCIO pin that can be supplied by between 3V to 5V.This allows each channel 's output voltage drive level to be individually configured. Thus allowing, for example 3.3V logic to be interfaced to the device without the need for external level converter I.C.'s.
- **Improved power management control for high- power USB Bus Powered devices**
  The PWREN# pin will become active when the device is enumerated by USB, and be deactivated when the device is in USB suspend. This can be used to directly drive a transistor or P-Channel MOSFET in applications where power switching of external circuitry is required. The BM pull down enable feature (configured in the external EPROM) is also retained. This will make the device gently pull down on the FIFO /UART IO lines when the power is shut off (PWREN# is high). In this mode any residual voltage on external circuitry is bled to GND when power is removed, thus ensuring that external circuitry controlled by PWREN# resets reliably when power is restored.
- **Support for Isochronous USB Transfers**
  Whilst USB Bulk transfer is usually the best choice for data transfer, the scheduling time of the data is not guaranteed. For applications where scheduling latency takes priority over data integrity such as transferring audio and low bandwidth video data, the FT2232C offers the option of USB Isochronous transfer via configuration of bit in the EEPROM.
- **Send Immediate /Wake Up Signal Pin on each channel**
  There is a Send Immediate /Wake Up (SI/WU) signal pins on each of the chips channels. These combine two functions on one pin. If USB is in suspend mode (and remote wakeup is enabled in the EEPROM), strobing this pin low will cause the device to request a resume from suspend (WakeUp) on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation, if this pin is strobed low any data in the device RX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the packet size. This can be used to optimise USB transfer speed for some applications.
- **Low suspend current**
  The suspend current of the FT2232C is typically under 100 uA (excluding the 1.5K pull up resistor on USBDP) in USB suspend mode. This allows greater margin for peripherals to meet the USB Suspend current limit of 500uA.
- **Programmable Receive Buffer Timeout**
  The TX buffer timeout is programmable over USB in 1ms increments from 1ms to 255ms,thus allowing the device to be better optimised for protocols requiring faster response times from short data packets.
- **Relaxed VCC Decoupling**
  The improved level of Vcc decoupling that was incorporated into BM devices has also been implemented in the FT2232C device.
- **Baud Rate Pre-Scaler Divisors**
  The FT2232C (UART mode) baud rate pre-scaler supports division by (n+0), (n+0.125), (n+0.25), (n+0.375), (n+0.5), (n+0.625), (n+0.75) and (n+0.875) where n is an integer between 2 and 16,384 (214).
- **Extended EEPROM Support**
  The FT2232C supports 93C46 (64 x 16 bit), 93C56 (128 x 16 bit), and 93C66 (256 x 16 bit) EEPROMs. The extra space is not used by the device, however it is available for use by other external MCU /logic whilst the FT2232C is being held in reset. There is now an additional 64 bytes of word of space available (128 bytes total) in the user area when a 93C56 or 93C66 is used.
- **USB 2.0 (full speed option)**
  An EEPROM based option allows the FT2232C to return a USB 2.0 device descriptor as opposed to USB 1.1.

Note: The device would be a USB 2.0 Full Speed device (12Mb/s) as opposed to a USB 2.0 High Speed device (480Mb/s).

In addition to the BM chip features, the FT2232C incorporates the following new features and interface modes: -

- **Enhanced Asynchronous Bit-Bang Interface**
  The FT2232C supports FTDI 's BM chip Bit Bang mode. In Bit Bang mode, the eight FIFO data lines can be switched between FIFO interface mode and an 8-bit Parallel IO port. Data packets can be sent to the device and they will be sequentially sent to the interface at a rate controlled by an internal timer (equivalent to the baud rate prescaler). With the FT2232C device this mode has been enhanced so that the internal RD# and WR# strobes are now brought out of the device which can be used to allow external logic to be clocked by accesses to the Bit-Bang IO bus.
- **Synchronous Bit-Bang Interface**
  With Synchronous Bit-Bang Mode the device is only read when it is written to, as opposed to asynchronously by the data rate generator. This makes it easier for the controlling program to measure the response to an output stimulus, as the data returned is synchronous to the output data.
- **High Output Drive Level Capability**
  The IO interface pins can be made to drive out at three times the standard drive level thus allowing multiple devices, or devices that require a greater drive strength to be interfaced to the FT2232C.This option is configured in the external EEPROM, and can be set individually for each channel.
- **CPU-Style FIFO Interface**
  The CPU style FIFO interface is essentially the same function as the classic FT245 interface, however the bus signals have been redefined to make them easier to interface to a CPU bus.
- **MCU Host Bus Emulation**
  This new mode combines the 'A' and 'B' bus interface to make the FT2232C interface emulates a standard 8048 /8051 style MCU bus. This allows peripheral devices for these MCU families to be directly attached to the FT2232C with IO being performed over USB with the help of MPSSE interface technology.
- **Multi-Protocol Synchronous Serial Engine Interface (M.P.S.S.E.)**
  The Multi-Protocol Synchronous Serial Engine (MPSSE) interface is a new option designed to interface efficiently with synchronous serial protocols such as JTAG and SPI Bus. It is very flexible in that it can be configured for different industry standards, or proprietary bus protocols. For instance, it is possible to connect one of the FT2232C 's channels to an SRAM configurable FPGA as supplied by vendors such as Altera and Xilinx. The FPGA device would normally be un-configured (i.e. have no defined function) at power-up. Application software on the PC could use the MPSSE to download configuration data to the FPGA over USB. This data would define the hardware 's function on power up. The other FT2232 channel would be available for other devices. This approach would allow a customer to create a "generic " USB peripheral; who 's hardware function can be defined under control of the application software. The FPGA based hardware could be easily upgraded or totally changed simply by changing the FPGA configuration data file. (See FTDI 's MORPH- IC development module for a practical example, www.morph-ic.com)
- **Fast Opto-Isolated Serial Interface**
  A new proprietary FTDI protocol is designed to allow galvanically isolated devices to communicate synchronously with the FT2232C using just 4 signal wires (over two dual opto-isolators),and two power lines. The peripheral circuitry controls the data transfer rate in both directions, whilst maintaining full data integrity. Maximum USB full speed data rates can be achieved. Both 'A' and 'B' channels can communicate over the same 4 wire interface if desired.

For further information regarding the FTDI FT2232C Multi-Purpose UART /FIFO controllers IC please refer to the FT2232C Datasheet. This datasheet can be found on the Elexol website at **http://www.elexol.com**

As mentioned above in module features, the USBMOD5 is in a 40-pin Dual In-Line Package. This allows the module to fit into a standard 40-pin 600mil IC Socket, which makes the module ideal for prototyping and development work. Shown in Diagram 2 below is the pin out for the USBMOD5.

USBMOD5 PINOUT

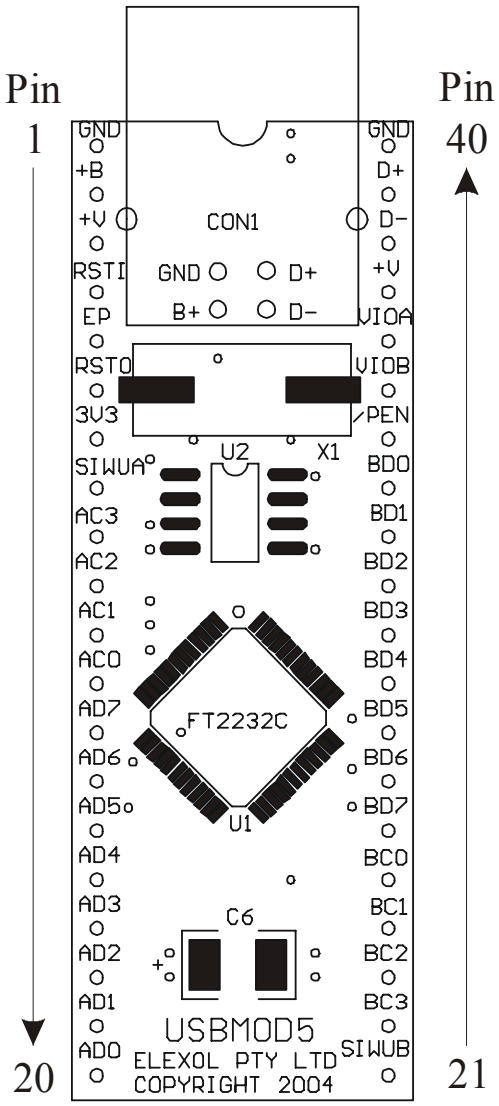


DIAGRAM 2

The following pin out table shows what the various pins are on the module.

USBMOD5 PINOUT TABLE

PIN #	SIGNAL	TYPE	DESCRIPTION
1	GND	PWR	Device – Ground Supply Pin
2	+B	PWR	USB Bus Power
3	+V	PWR	Device - +4.4 volt to +5.25 volt Power Supply Pin
4	RSTI	IN	Can be used by external device to reset chip. If not required tie to VCC
5	EP**	IN	Enumeration Power connect to RSTO for bus powered operation or 3V3 to instruct PC to connect to device
6	RSTO	OUT	Output of the internal Reset Generator. Stays high impedance for ~2ms after VCC >3.5v and the internal clock starts up, then clamps it 's output to the 3.3v output of the internal regulator. Taking RSTI low will also force RSTO to go high impedance. RSTO is NOT affected by a USB Bus Reset.
7	3V3	OUT	3.3 volt Output from the integrated L.D.O. regulator. This pin should be decoupled to GND using a 33nF ceramic capacitor in close proximity to the device pin. Its prime purpose is to provide the internal 3.3v supply to the USB transceiver cell and the RSTO pin. A small amount of current (<=5mA) can be drawn from this pin to power external 3.3v logic if required.
8-33	Channel A&B	IN	See following table for description of I/O pin configuration in various chip modes
34	/PEN	OUT	Goes Low after the device is configured via USB, then high during USB suspend. Can be used to control power to external logic using a P-Channel Logic Level MOSFET Switch. Enable the Interface Pull-Down Option in EEPROM when using the /PEN pin this way.
35	VIOB**	PWR	+3.0 volt to +5.25 volt VCC to the UART interface pins 10..12,14..16 and 18..25. When interfacing with 3.3v external logic connect VIO to the 3.3v supply of the external logic, otherwise connect to +V to drive out at 5v CMOS level.
36	VIOA**	PWR	+3.0 volt to +5.25 volt VCC to the UART interface pins 10..12,14..16 and 18..25. When interfacing with 3.3v external logic connect VIO to the 3.3v supply of the external logic, otherwise connect to +V to drive out at 5v CMOS level.
37	+V	PWR	Device - +4.4 volt to +5.25 volt Power Supply Pin
38	D-	I/O	USB Data Signal Minus
39	D+	I/O	USB Data Signal Plus
40	GND	PWR	Device – Ground Supply Pin

** **Note 1** – When connecting the USBMOD5 to the USB tie EP (pin 5) to RSTO (pin 6) so that the unit can enumerate.

** **Note 2** – Tie VIOA (pin 36) and VIOB (pin 35) to V+ (pin 37) to drive the FIFO pins to 5V CMOS Level

USBMOD5 PINOUT TABLE Continued

PIN #	SIGNAL	DESCRIPTION by Chip Mode **Note 2						
		232 UART Mode	245 FIFO Mode	CPU FIFO Interface	Enhanced Asynchronous and Synchronous Bit Bang Modes	MPSSE **Note 4	MCU Host Bus Emulation Mode	Fast Opto Isolated Serial Mode
8	SIWUA	SI/WUA	SI/WUA	**Note 8	SI/WUA	**Note 8	**Note 8	**Note 3
9	AC3	TXLED#	WR	WR#	RD# **Note 7	GPIOH3	OSC	-
10	AC2	RXLED#	RD#	RD#	WR# **Note 7	GPIOH2	IORDY	-
11	AC1	SLEEP#	TXE#	A0	RD# **Note 6	GPIOH1	I/O 1	-
12	AC0	TXDEN	RXF#	CS#	WR# **Note 6	GPIOH0	I/O 0	-
13	AD7	RI#	D7	D7	D7	GPIOL3	AD7	-
14	AD6	DCD#	D6	D6	D6	GPIOL2	AD6	-
15	AD5	DSR#	D5	D5	D5	GPIOL1	AD5	-
16	AD4	DTR#	D4	D4	D4	GPIOL0	AD4	-
17	AD3	CTS#	D3	D3	D3	TMS/CS	AD3	-
18	AD2	RTS#	D2	D2	D2	TDO/DI	AD2	-
19	AD1	RXD	D1	D1	D1	TDI/D0	AD1	-
20	AD0	TXD	D0	D0	D0	TCK/SK	AD0	-
21	SIWUB	SI/WUB	SI/WUB	**Note 8	SI/WUB	**Note 8	**Note 8	**Note 3
22	BC3	TXLED#	WR	WR#	RD# **Note 7	-	WR#	-
23	BC2	RXLED#	RD#	RD#	WR# **Note 7	-	RD#	-
24	BC1	SLEEP#	TXE#	A0	RD# **Note 6	-	ALE	-
25	BC0	TXDEN	RXF#	CS#	WR# **Note 6	-	CS#	-
26	BD7	RI#	D7	D7	D7	-	AD15	-
27	BD6	DCD#	D6	D6	D6	-	AD14	-
28	BD5	DSR#	D5	D5	D5	-	AD13	-
29	BD4	DTR#	D4	D4	D4	-	AD12	**Note 3
30	BD3	CTS#	D3	D3	D3	-	AD11	FSCTS
31	BD2	RTS#	D2	D2	D2	-	AD10	FSDO
32	BD1	RXD	D1	D1	D1	-	AD9	FSCLK
33	BD0	TXD	D0	D0	D0	-	AD8	FSDI

Note 2: 232 UART, 245 FIFO, CPU FIFO Interface, and Fast Opto-Isolated modes are enabled in the external EEPROM. Enhanced Asynchronous and Synchronous Bit-Bang modes, MPSSE, and MCU Host Bus Emulation modes are enabled using driver commands.

Note 3: Channel A can be configured in another IO mode if channel B is in Fast Opto-Isolated Serial Mode. If both Channel A and Channel B are in Fast Opto-Isolated Serial Mode all of the IO will be on Channel B.

Note 4: MPSSE is Channel A only.

Note 5: MCU Host Bus Emulation requires both Channels.

Note 6: The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 245 FIFO, CPU FIFO interface, or Fast Opto-Isolated Serial Modes.

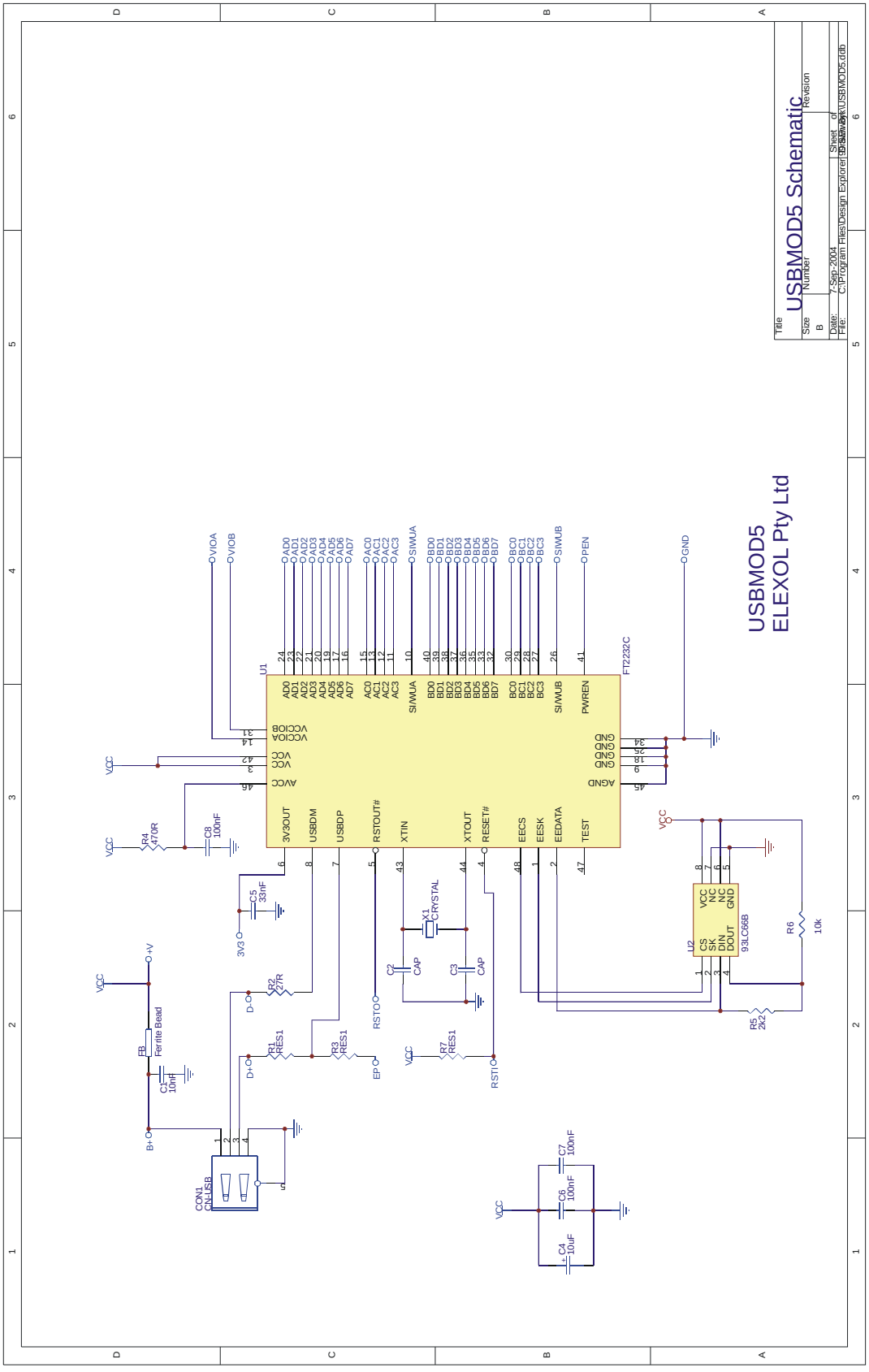
Note 7: The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 232 UART Mode.

Note 8: SI/WU is not available in these modes.

Note 9: The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 245 FIFO, CPU FIFO interface. Bit-Bang mode is not available on Channel B when Fast Opto-Isolated Serial Mode is enabled.

The following page shows the schematic for the USBMOD5.

USBMOD5 SCHEMATIC



Driver Installation

To install the FT2232C drivers, download the driver from the FTDI website http://www.ftdichip.com and unzip the files to a local directory on the PC.

Connect the USBMOD5 and windows will recognise the device and automatically ask for the location of the driver. If the computer doesn't ask for the driver's location, check that the necessary pins are connected together. There is a Note provided under the pin out table in the datasheet for pins to connect together. Select *specify a location* and *browse* to the directory where you have unzipped the files.

There are two types of drivers that the PC can install, they are:

1. ***VCP*** (Virtual COM Port) – appears to the PC as an extra Com Port together with any existing hardware Com Ports. The Virtual COM Port is accessed in the same way as a standard Windows COM Port using window API calls or by using a COM Port Library

2. ***Direct DLL*** – interfaces using a DLL instead of the VCP. Programming with the Direct DLL driver is by calls to the DLL Library functions that can be done with a number of different development languages (VC++, C++ Builder, Delphi, VB etc....). More information about programming with the Direct DLL driver can be found in the D2XX Programmers guide which is available for download from the FTDI website

The driver that the PC will install depends on the software option that is set in the EEPROM. The options that are set into the external EEPROM on the USBMOD5 at ELEXOL are:

- Chip mode
  - Channel A – 232 UART Mode
  - Channel B – 232 UART Mode
- Software option
  - Channel A – VCP
  - Channel B – VCP

To change the chip modes or software options, use the MPROG 2 EEPROM Programmer. This program is available for download from the FTDI website.

Document Revision History

USBMOD5 Datasheet Version 1.0 – Initial document created 21th April 2005

USBMOD5 Datasheet Version 1.1 – Updated 29th June 2005

- **Note 1 on pin table changed due to wrong pin allocation**

Absolute Maximum Ratings

Storage Temperature ..... -65°C to + 150°C
Ambient Temperature (Power Applied) ..... 0°C to + 70°C
VCC Supply Voltage ..... -0.5v to +6.00v
DC Input Voltage - Inputs..... -0.5v to VCC + 0.5v
DC Input Voltage - High Impedance Bidirectionals..... -0.5v to VCC + 0.5v
DC Output Current – Outputs 24mA
DC Output Current – Low Impedance Bidirectionals 24mA
Power Dissipation 500mW

DC Characteristics (Ambient Temperature = 0°C .. 70°C)

Operating Voltage and Current

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
Vcc1	+V Operating Supply Voltage	4.4	5.0	5.25	V	
Vcc2	VIO Operating Supply Voltage	3.0	-	5.25	V	
Icc1	Operating Supply Current	-	30	-	mA	Normal Operation
Icc2	Operating Supply Current	-	100	200	uA	USB Suspend ****Note 10**

**** Note 10** – Supply current excludes the 200uA nominal drawn by the external pull up resistor on USBDP

I/O Pin Characteristics (VCCIO = 5V, Standard Drive Level) **Note 11

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 2 mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 2 mA
Vin	Input Switching Threshold	1.3	1.6	1.9	V	
VHys	Input Switching Hysteresis	50	55	60	mV	

I/O Pin Characteristics (VCCIO = 3.3V, Standard Drive Level) **Note11

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
Voh	Output Voltage High	2.2	2.7	3.2	V	I source = 1 mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2 mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	
VHys	Input Switching Hysteresis	20	25	30	mV	

**** Note 11** – Inputs have an internal 200kΩ pull-up resistor to VCCIO, which can alternatively be programmed to pull down using a configuration bit in the external EEPROM

RSTI Pin Characteristics **Note 12

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 2 mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2 mA
Vin	Input Switching Threshold	1.3	1.6	1.9	V	
VHys	Input Switching Hysteresis	50	55	60	mV	

**** Note 12** – RSTI pin have an internal 200kΩ pull-up resistor to +V

RSTO Pin Characteristics

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
Voh	Output Voltage High	3.0	-	3.6	V	I source = 2 mA
Vol	Output Voltage Low	0.3	-	0.6	V	I source = 2 mA

USB I/O Pin Characteristics **Note 13

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
UVoh	I/O Pins Static Output (High)	2.8	-	3.6	V	Rl = 1.5kΩ to 3V3Out (D+) Rl = 15kΩ to GND (D+)
UVol	I/O Pin Static Output (Low)	0	-	0.3	V	Rl = 1.5kΩ to 3V3Out (D+) Rl = 15kΩ to GND (D+)
UVse	Single Ended RX Threshold	0.8		2.0	V	
UCom	Differential Common Mode	0.8		2.5	V	
UVDif	Differential Input Sensitivity	0.2			V	
UDrvZ	Driver Output Impedance	29		44	Ω (ohm)	

**** Note 13** – Driver Output Impedance includes the external 27Ω series resistors on D+ and D- pins.

Technical Support and Further Information

For any questions relating to the USBMOD5 please contact us by Email:
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Product Use Limitations, Warranty and Quality Statement.

The USBMOD5 should not be used in any situation where it's failure or failure of the PC or software controlling it could cause human injury or severe damage to equipment.
This device is not designed for or intended to be used in any life critical application.

The USBMOD5 is warranted to be free from manufacture defects for a period of 12 months from the date purchase.
Subjecting the device to conditions beyond the Absolute Maximum Ratings listed above will invalidate this warranty.
The USBMOD5 is a static sensitive device, anti static procedures should be used in the handling of this device.

All USBMOD5 units are tested during manufacture and are despatched free of defects.

Elexol is committed to providing products of the highest quality. Should you experience any product quality issues with this product please contact our quality assurance manager at the above address.

Disclaimer.

This product and its documentation are provided as-is and no warranty is made or implied as to their suitability for any particular purpose.
Elexol Pty Ltd will not accept any claim for damages arising from the use of this product or documentation.
This document provides information on our products and all efforts are made to ensure the accuracy of the information contained within. The specifications of the product are subject to change and continual improvement without notification.

Other than the extent permitted by law and subject to the Trade Practice Act, all and any liability for consequential loss or damage arising from an ELEXOL USBMOD5 is hereby limited, at ELEXOL's discretion, to replacement or repair.