



**Paragraph
Number**

TABLE OF CONTENTS

**Page
Number**

Section 1 INTRODUCTION

Section 2 NOMENCLATURE

2.1 Symbols and Operators	2-1
2.2 CPU32 Register Mnemonics	2-2
2.3 Register Mnemonics	2-2
2.4 Conventions	2-4

Section 3 OVERVIEW

3.1 MCU Features	3-1
3.1.1 Central Processor Unit (CPU32)	3-1
3.1.2 System Integration Module(SIM)	3-1
3.1.3 Queued Serial Module (QSM)	3-1
3.1.4 Time Processor Unit (TPU)	3-2
3.1.5 Static RAM Module with TPU Emulation Capability (TPURAM).	3-2
3.2 Intermodule Bus	3-2
3.3 System Block Diagram and Pin Assignment Diagrams	3-2
3.4 Pin Descriptions	3-6
3.5 Signal Descriptions	3-9
3.6 Internal Register Maps	3-14
3.7 Address Space Maps	3-14

Section 4 CENTRAL PROCESSOR UNIT

4.1 General	4-1
4.2 CPU32 Registers	4-2
4.2.1 Data Registers	4-4
4.2.2 Address Registers	4-5
4.2.3 Program Counter	4-6
4.2.4 Control Registers	4-6
4.2.4.1 Status Register	4-6
4.2.4.2 Alternate Function Code Registers	4-7
4.2.5 Vector Base Register (VBR)	4-7
4.3 Memory Organization	4-7
4.4 Virtual Memory	4-9
4.5 Addressing Modes	4-9
4.6 Processing States	4-9
4.7 Privilege Levels	4-10

**Paragraph
Number**

**Page
Number**



4.8 Instructions	4-10
4.8.1 M68000 Family Compatibility	4-14
4.8.2 Special Control Instructions	4-15
4.8.2.1 Low-Power Stop (LPSTOP)	4-15
4.8.2.2 Table Lookup and Interpolate (TBL)	4-15
4.8.2.3 Loop Mode Instruction Execution	4-15
4.9 Exception Processing	4-16
4.9.1 Exception Vectors	4-16
4.9.2 Types of Exceptions	4-17
4.9.3 Exception Processing Sequence	4-18
4.10 Development Support	4-18
4.10.1 M68000 Family Development Support	4-19
4.10.2 Background Debug Mode	4-19
4.10.3 Enabling BDM	4-20
4.10.4 BDM Sources	4-20
4.10.4.1 External $\overline{\text{BKPT}}$ Signal	4-21
4.10.4.2 BGND Instruction	4-21
4.10.4.3 Double Bus Fault	4-21
4.10.4.4 Peripheral Breakpoints	4-21
4.10.5 Entering BDM	4-21
4.10.6 BDM Commands	4-22
4.10.7 Background Mode Registers	4-23
4.10.7.1 Fault Address Register (FAR)	4-23
4.10.7.2 Return Program Counter (RPC)	4-23
4.10.7.3 Current Instruction Program Counter (PCC)	4-24
4.10.8 Returning from BDM	4-24
4.10.9 Serial Interface	4-24
4.10.10 Recommended BDM Connection	4-26
4.10.11 Deterministic Opcode Tracking	4-27
4.10.12 On-Chip Breakpoint Hardware	4-27

**Section 5
SYSTEM INTEGRATION MODULE**

5.1 General	5-1
5.2 System Configuration	5-2
5.2.1 Module Mapping	5-2
5.2.2 Interrupt Arbitration	5-2
5.2.3 Show Internal Cycles	5-3
5.2.4 Register Access	5-3
5.2.5 Freeze Operation	5-3
5.3 System Clock	5-4
5.3.1 Clock Sources	5-4
5.3.2 Clock Synthesizer Operation	5-5

**Paragraph
Number**

**Page
Number**



5.3.3	External Bus Clock	5-20
5.3.4	Low-Power Operation	5-20
5.4	System Protection	5-21
5.4.1	Reset Status	5-22
5.4.2	Bus Monitor	5-22
5.4.3	Halt Monitor	5-23
5.4.4	Spurious Interrupt Monitor	5-23
5.4.5	Software Watchdog	5-23
5.4.6	Periodic Interrupt Timer	5-25
5.4.7	Interrupt Priority and Vectoring	5-26
5.4.8	Low-Power STOP Mode Operation	5-27
5.5	External Bus Interface	5-27
5.5.1	Bus Control Signals	5-29
5.5.1.1	Address Bus	5-29
5.5.1.2	Address Strobe	5-29
5.5.1.3	Data Bus	5-29
5.5.1.4	Data Strobe	5-30
5.5.1.5	Read/Write Signal	5-30
5.5.1.6	Size Signals	5-30
5.5.1.7	Function Codes	5-30
5.5.1.8	Data and Size Acknowledge Signals	5-31
5.5.1.9	Bus Error Signal	5-31
5.5.1.10	Halt Signal	5-31
5.5.1.11	Autovector Signal	5-32
5.5.2	Dynamic Bus Sizing	5-32
5.5.3	Operand Alignment	5-33
5.5.4	Misaligned Operands	5-33
5.5.5	Operand Transfer Cases	5-34
5.6	Bus Operation	5-34
5.6.1	Synchronization to CLKOUT	5-34
5.6.2	Regular Bus Cycles	5-35
5.6.2.1	Read Cycle	5-36
5.6.2.2	Write Cycle	5-37
5.6.3	Fast Termination Cycles	5-38
5.6.4	CPU Space Cycles	5-38
5.6.4.1	Breakpoint Acknowledge Cycle	5-39
5.6.4.2	LPSTOP Broadcast Cycle	5-42
5.6.5	Bus Exception Control Cycles	5-42
5.6.5.1	Bus Errors	5-44
5.6.5.2	Double Bus Faults	5-44
5.6.5.3	Retry Operation	5-45
5.6.5.4	Halt Operation	5-45
5.6.6	External Bus Arbitration	5-46

**Paragraph
Number**

**Page
Number**



5.6.6.1 Show Cycles.....	5-47
5.7 Reset.....	5-48
5.7.1 Reset Exception Processing.....	5-48
5.7.2 Reset Control Logic.....	5-48
5.7.3 Reset Mode Selection.....	5-49
5.7.3.1 Data Bus Mode Selection.....	5-50
5.7.3.2 Clock Mode Selection.....	5-53
5.7.3.3 Breakpoint Mode Selection.....	5-53
5.7.4 MCU Module Pin Function During Reset.....	5-53
5.7.5 Pin States During Reset.....	5-54
5.7.5.1 Reset States of SIM Pins.....	5-54
5.7.5.2 Reset States of Pins Assigned to Other MCU Modules.....	5-55
5.7.6 Reset Timing.....	5-56
5.7.7 Power-On Reset.....	5-56
5.7.8 Use of the Three-State Control Pin.....	5-57
5.7.9 Reset Processing Summary.....	5-58
5.7.10 Reset Status Register.....	5-58
5.8 Interrupts.....	5-58
5.8.1 Interrupt Exception Processing.....	5-59
5.8.2 Interrupt Priority and Recognition.....	5-59
5.8.3 Interrupt Acknowledge and Arbitration.....	5-60
5.8.4 Interrupt Processing Summary.....	5-61
5.8.5 Interrupt Acknowledge Bus Cycles.....	5-62
5.9 Chip-Selects.....	5-62
5.9.1 Chip-Select Registers.....	5-65
5.9.1.1 Chip-Select Pin Assignment Registers.....	5-65
5.9.1.2 Chip-Select Base Address Registers.....	5-66
5.9.1.3 Chip-Select Option Registers.....	5-67
5.9.1.4 Port C Data Register.....	5-68
5.9.2 Chip-Select Operation.....	5-68
5.9.3 Using Chip-Select Signals for Interrupt Acknowledge.....	5-69
5.9.4 Chip-Select Reset Operation.....	5-70
5.10 Parallel Input/Output Ports.....	5-72
5.10.1 Pin Assignment Registers.....	5-72
5.10.2 Data Direction Registers.....	5-72
5.10.3 Data Registers.....	5-72
5.11 Factory Test.....	5-73

**Section 6
QUEUED SERIAL MODULE**

6.1 General.....	6-1
6.2 QSM Registers and Address Map.....	6-2
6.2.1 QSM Global Registers.....	6-2

**Paragraph
Number**

**Page
Number**



6.2.1.1	Low-Power Stop Mode Operation	6-2
6.2.1.2	Freeze Operation	6-3
6.2.1.3	QSM Interrupts	6-3
6.2.2	QSM Pin Control Registers	6-4
6.3	Queued Serial Peripheral Interface	6-5
6.3.1	QSPI Registers	6-7
6.3.1.1	Control Registers	6-7
6.3.1.2	Status Register	6-8
6.3.2	QSPI RAM	6-8
6.3.2.1	Receive RAM	6-8
6.3.2.2	Transmit RAM	6-9
6.3.2.3	Command RAM	6-9
6.3.3	QSPI Pins	6-9
6.3.4	QSPI Operation	6-9
6.3.5	QSPI Operating Modes	6-10
6.3.5.1	Master Mode	6-18
6.3.5.2	Master Wrap-Around Mode	6-21
6.3.5.3	Slave Mode	6-22
6.3.5.4	Slave Wrap-Around Mode	6-23
6.3.6	Peripheral Chip-Selects	6-23
6.4	Serial Communication Interface	6-23
6.4.1	SCI Registers	6-24
6.4.1.1	Control Registers	6-24
6.4.1.2	Status Register	6-27
6.4.1.3	Data Register	6-27
6.4.2	SCI Pins	6-27
6.4.3	SCI Operation	6-27
6.4.3.1	Definition of Terms	6-27
6.4.3.2	Serial Formats	6-28
6.4.3.3	Baud Clock	6-28
6.4.3.4	Parity Checking	6-29
6.4.3.5	Transmitter Operation	6-29
6.4.3.6	Receiver Operation	6-31
6.4.3.7	Idle-Line Detection	6-32
6.4.3.8	Receiver Wake-up	6-32
6.4.3.9	Internal Loop Mode	6-33

**Section 7
TIME PROCESSOR UNIT**

7.1	General	7-1
7.2	TPU Components	7-2
7.2.1	Time Bases	7-2
7.2.2	Timer Channels	7-2

**Paragraph
Number**

**Page
Number**



7.2.3 Scheduler	7-3
7.2.4 Microengine	7-3
7.2.5 Host Interface	7-3
7.2.6 Parameter RAM	7-3
7.3 TPU Operation	7-3
7.3.1 Event Timing	7-4
7.3.2 Channel Orthogonality	7-4
7.3.3 Interchannel Communication	7-4
7.3.4 Programmable Channel Service Priority	7-4
7.3.5 Coherency	7-4
7.3.6 Emulation Support	7-5
7.3.7 TPU Interrupts	7-5
7.4 A Mask Set Time Functions	7-6
7.4.1 Discrete Input/Output (DIO)	7-6
7.4.2 Input Capture/Input Transition Counter (ITC)	7-6
7.4.3 Output Compare (OC)	7-7
7.4.4 Pulse-Width Modulation (PWM)	7-7
7.4.5 Synchronized Pulse-Width Modulation (SPWM)	7-7
7.4.6 Period Measurement with Additional Transition Detect (PMA)	7-7
7.4.7 Period Measurement with Missing Transition Detect (PMM)	7-8
7.4.8 Position-Synchronized Pulse Generator (PSP)	7-8
7.4.9 Stepper Motor (SM)	7-9
7.4.10 Period/Pulse-Width Accumulator (PPWA)	7-9
7.4.11 Quadrature Decode (QDEC)	7-10
7.5 G Mask Set Time Functions	7-10
7.5.1 Table Stepper Motor (TSM)	7-10
7.5.2 New Input Capture/Transition Counter (NITC)	7-11
7.5.3 Queued Output Match (QOM)	7-11
7.5.4 Programmable Time Accumulator (PTA)	7-11
7.5.5 Multichannel Pulse-Width Modulation (MCPWM)	7-11
7.5.6 Fast Quadrature Decode (FQD)	7-12
7.5.7 Universal Asynchronous Receiver/Transmitter (UART)	7-12
7.5.8 Brushless Motor Commutation (COMM)	7-12
7.5.9 Frequency Measurement (FQM)	7-13
7.5.10 Hall Effect Decode (HALLD)	7-13
7.6 Host Interface Registers	7-13
7.6.1 System Configuration Registers	7-13
7.6.1.1 Prescaler Control for TCR1	7-13
7.6.1.2 Prescaler Control for TCR2	7-14
7.6.1.3 Emulation Control	7-15
7.6.1.4 Low-Power Stop Control	7-15
7.6.2 Channel Control Registers	7-15
7.6.2.1 Channel Interrupt Enable and Status Registers	7-15

**Paragraph
Number**

**Page
Number**



7.6.2.2 Channel Function Select Registers	7-16
7.6.2.3 Host Sequence Registers	7-17
7.6.2.4 Host Service Registers	7-17
7.6.2.5 Channel Priority Registers	7-17
7.6.3 Development Support and Test Registers	7-17

**Section 8
STANDBY RAM WITH TPU EMULATION**

8.1 General	8-1
8.2 TPURAM Register Block	8-1
8.3 TPURAM Array Address Mapping	8-1
8.4 TPURAM Privilege Level	8-2
8.5 Normal Operation	8-2
8.6 Standby Operation	8-2
8.7 Low-Power Stop Operation	8-3
8.8 Reset	8-3
8.9 TPU Microcode Emulation	8-3

**Appendix A
ELECTRICAL CHARACTERISTICS**

**Appendix B
MECHANICAL DATA AND ORDERING INFORMATION**

B.1 Obtaining Updated MC68332 Mechanical Information	B-7
B.2 Ordering Information	B-7

**Appendix C
DEVELOPMENT SUPPORT**

C.1 M68MMDS1632 Modular Development System	C-1
C.2 M68MEVB1632 Modular Evaluation Board	C-1

**Appendix D
REGISTER SUMMARY**

D.1 Central Processor Unit	D-1
D.1.1 CPU32 Register Model	D-2
D.1.2 Status Register	D-3
D.2 System Integration Module	D-5
D.2.1 SIM Configuration Register	D-6
D.2.2 System Integration Test Register	D-8
D.2.3 Clock Synthesizer Control Register	D-8
D.2.4 Reset Status Register	D-9
D.2.5 System Integration Test Register (ECLK)	D-9
D.2.6 Port E Data Register	D-10
D.2.7 Port E Data Direction Register	D-10
D.2.8 Port E Pin Assignment Register	D-10
D.2.9 Port F Data Register	D-11
D.2.10 Port F Data Direction Register	D-11
D.2.11 Port F Pin Assignment Register	D-12

**Paragraph
Number**

**Page
Number**



D.2.12	System Protection Control Register	D-12
D.2.13	Periodic Interrupt Control Register.	D-13
D.2.14	Periodic Interrupt Timer Register.	D-14
D.2.15	Software Watchdog Service Register	D-15
D.2.16	Port C Data Register	D-15
D.2.17	Chip-Select Pin Assignment Registers	D-15
D.2.18	Chip-Select Base Address Register Boot ROM.	D-17
D.2.19	Chip-Select Base Address Registers.	D-17
D.2.20	Chip-Select Option Register Boot ROM.	D-18
D.2.21	Chip-Select Option Registers.	D-18
D.2.22	Master Shift Registers	D-21
D.2.23	Test Module Shift Count Register	D-21
D.2.24	Test Module Repetition Count Register.	D-21
D.2.25	Test Submodule Control Register	D-22
D.2.26	Distributed Register	D-22
D.3	Standby RAM Module with TPU Emulation Capability (TPURAM)	D-22
D.3.1	TPURAM Module Configuration Register	D-22
D.3.2	TPURAM Test Register	D-23
D.3.3	TPURAM Module Configuration Register	D-23
D.4	Queued Serial Module.	D-23
D.4.1	QSM Configuration Register	D-24
D.4.2	QSM Test Register	D-25
D.4.3	QSM Interrupt Level Register	D-25
D.4.4	QSM Interrupt Vector Register.	D-26
D.4.5	SCI Control Register	D-27
D.4.7	SCI Status Register	D-29
D.4.8	SCI Data Register	D-30
D.4.9	Port QS Data Register	D-30
D.4.10	Port QS Pin Assignment Register/Data Direction Register	D-31
D.4.11	QSPI Control Register 0	D-32
D.4.12	QSPI Control Register 1	D-34
D.4.13	QSPI Control Register 2	D-35
D.4.14	QSPI Control Register 3	D-36
D.4.15	QSPI Status Register.	D-37
D.4.16	Receive Data RAM	D-37
D.4.17	Transmit Data RAM	D-38
D.4.18	Command RAM	D-38
D.5	Time Processor Unit (TPU)	D-39
D.5.1	TPU Module Configuration Register	D-40
D.5.2	Test Configuration Register	D-41
D.5.3	Development Support Control Register	D-41
D.5.4	Development Support Status Register.	D-42
D.5.5	TPU Interrupt Configuration Register.	D-43
D.5.6	Channel Interrupt Enable Register.	D-44
D.5.7	Channel Function Select Registers	D-44
D.5.8	Host Sequence Registers	D-45
D.5.9	Host Service Request Registers	D-45
D.5.10	Channel Priority Registers	D-46
D.5.11	Channel Interrupt Status Register	D-46
D.5.12	Link Register	D-46
D.5.13	Service Grant Latch Register.	D-47
D.5.14	Decoded Channel Number Register	D-47
D.5.15	TPU Parameter RAM	D-47

**Paragraph
Number**

INDEX

**Page
Number**



Online publishing by JABIS™, <http://www.jabis.com>

**Paragraph
Number**

**Page
Number**

