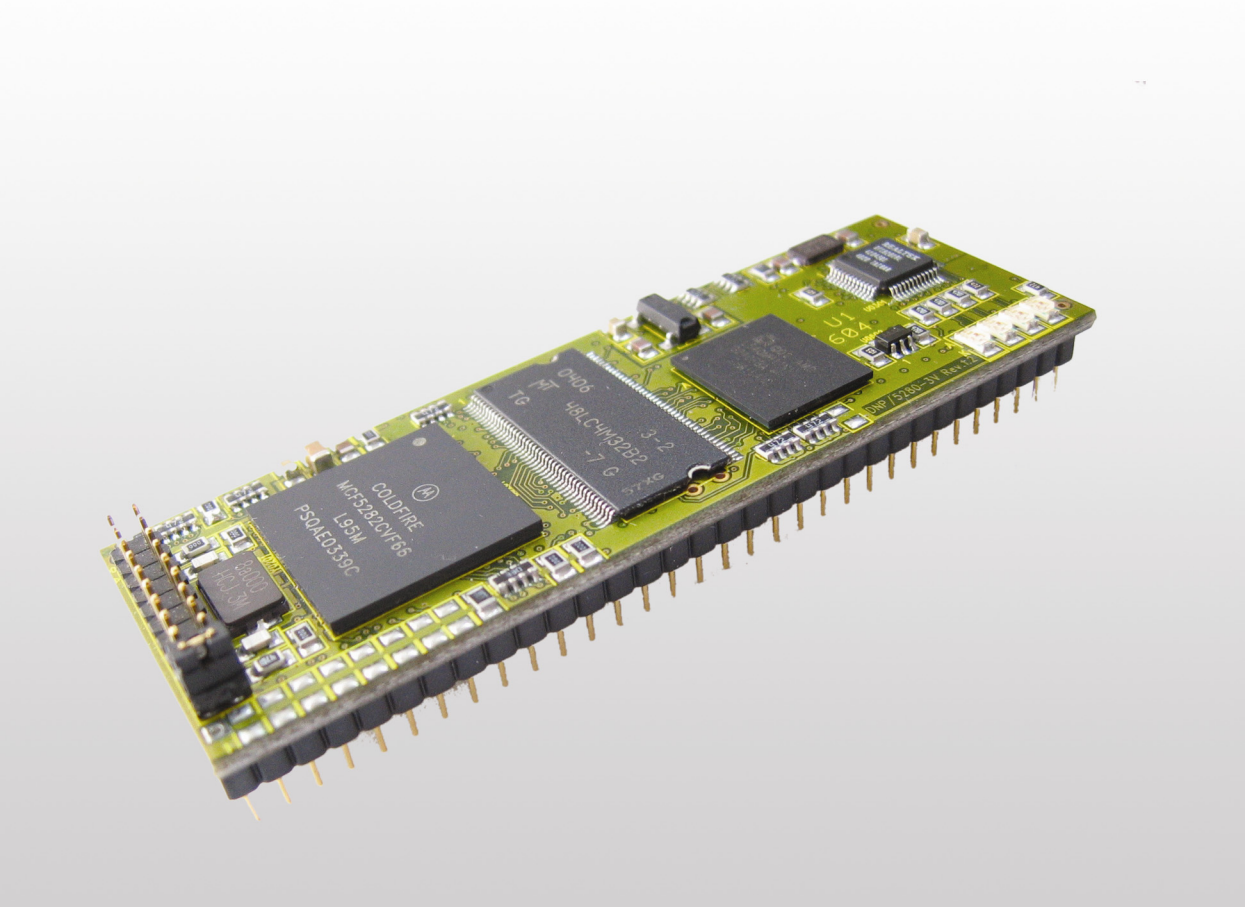
DIL/NetPC DNP/5280
Board Revision 1.2

Hardware Reference



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For further information regarding our products please visit us at www.dilnetpc.com

CONTENT

1 INTRODUCTION

Thank you for choosing a SSV Product. We are confident that you will be pleased with the performance of your product. Please take a few minutes to read this manual.

For further information about the individual components you may follow the links from our website at: *http://www.dilnetpc.com*

Our Website contains a lot of technical information, which will be updated in regular periods.

1.1 Block Diagram

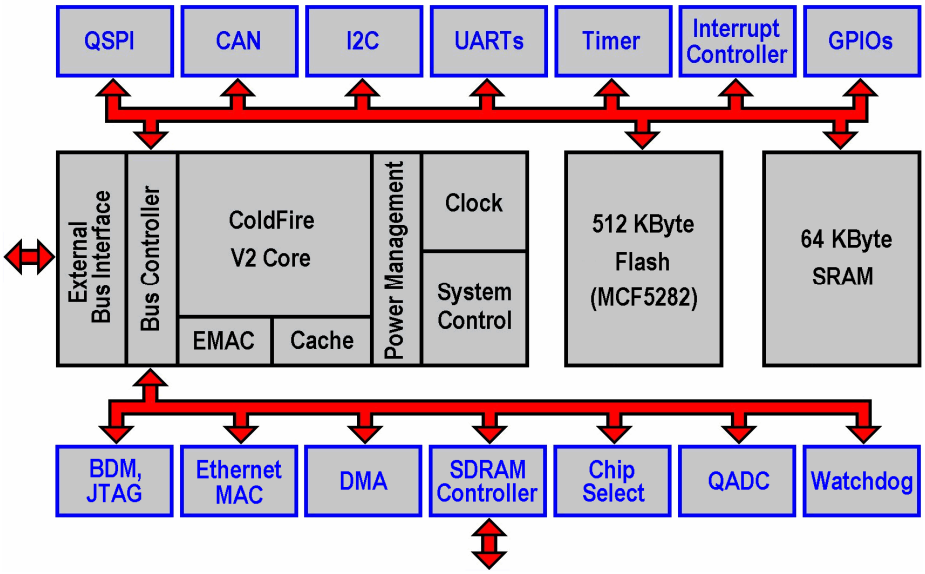


Figure 1-1: Block Diagram of the MCF5280/MCF5282-Microcontroller

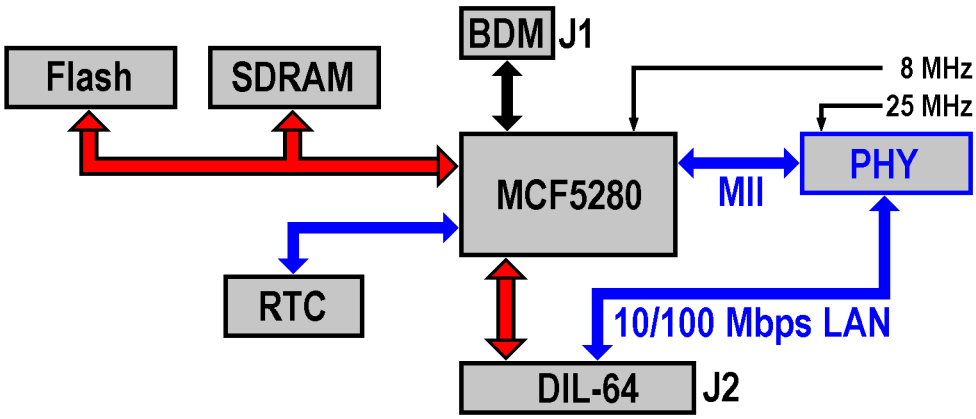
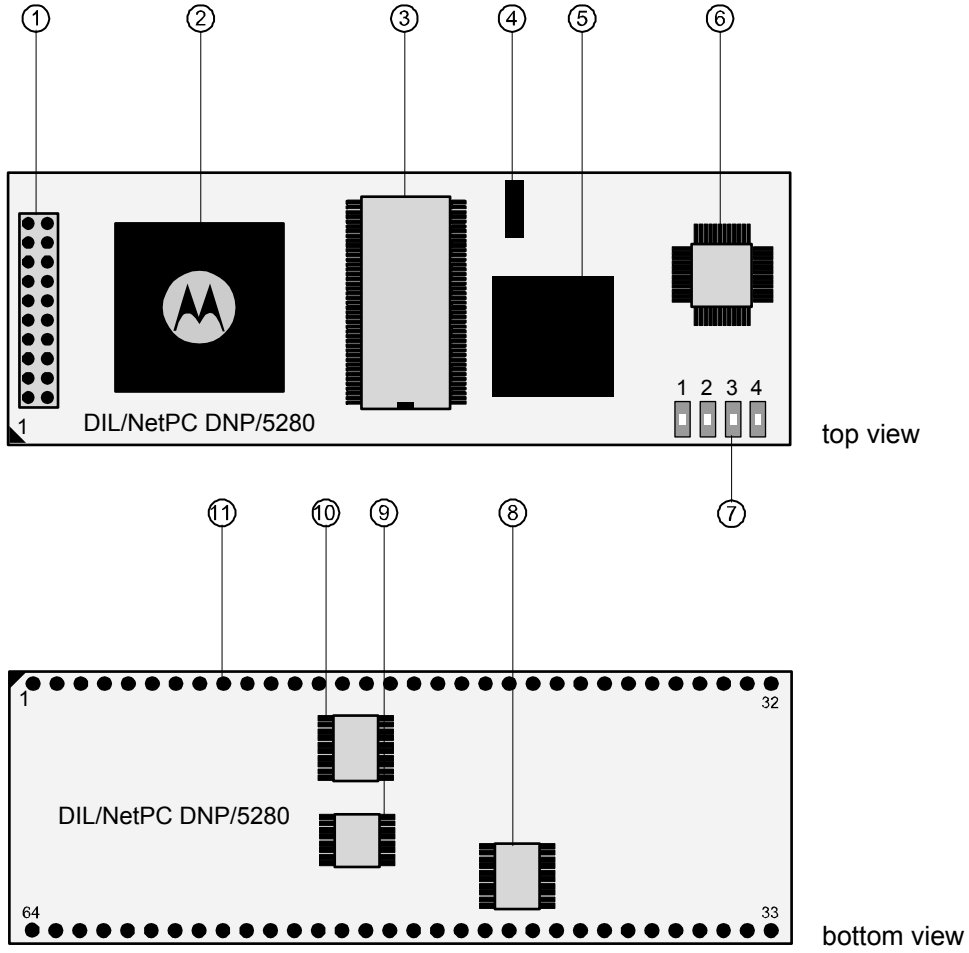


Figure 1-2: Block Diagram of the DNP/5280

1.2 Features

- Motorola 32-bit MCF5282 ColdFire with 66 MHz Clock Speed
- 63 MIPS (Dhrystone 2.1)
- 16 MByte SDRAM Memory, 8 MByte FLASH Memory
- 10/100 Mbps Ethernet LAN Interface
- Four LAN Status LEDs
- Two asynchronous Serial Ports (one with all Handshakes)
- One I2C Interchip Bus Interface
- One Queued Serial Peripheral Interface (SPI)
- One CAN Interface (Supports CAN Protocol Specification 2.0B)
- 20-bit General Purpose high-speed Parallel I/O
- 8-bit I/O Expansion Bus
- Five Interrupt Inputs
- Four Chip Select Outputs
- Programmable General Purpose Timers and Watchdog Timer
- Motorola BDM (Background Debug Mode) Interface for In-Circuit Debugging
- In-System Programming Features
- 64-pin JEDEC DIL-64 Connector, 2.54mm Centers
- 3.3 Volt Low Power Design, Supply Voltage 3.3 VDC (± 5%)
- Supply Current 300 mA typ. at 66 MHz
- Size 82mm x 28mm

2 DNP/5280 OVERVIEW



① J1 - BDM interface
② MCF5282CVF66 CPU
③ SDRAM
④ 32KHz quartz
⑤ Flash memory
⑥ 10/100 Mbps Ethernet PHY
⑦ LAN activity LEDs
⑧ RTC DS1306
⑨ TTL
⑩ TTL
⑪ J2 - 64-pin DIL connector

Figure 2-1: OverviewDNP/5280

3 DNP/5280 COMPONENTS

This chapter describes components of the DIL/NetPC DNP/5280 shown in **chapter 2** and gives a short overview about their respective functions.

3.1 J1 – BDM Interface

The BDM (Background Debug Mode) interface offers in-circuit debugging. Through a special adapter cable the Flash memory is in-system programmable.

Please refer to **chapter 4.6** for the complete pinout.

3.2 MCF5282CVF66 CPU

The DNP/5280 provides a very compact ColdFire-based low power embedded controller (Motorola 32-bit MCF5282CVF66) with TCP/IP stack and web server for high-speed embedded networking applications.

3.3 SDRAM

The capacity of the SDRAM memory chip is 16 MByte with a 32-bit data path.

3.4 32KHz Quartz

This 32KHz quartz is used by the RTC (real time clock).

3.5 Flash Memory

The boot block of the Flash memory is only in-system programmable over the Motorola BDM interface through a special adapter cable attached to a PC parallel port. For all other Flash blocks you can use also a high-speed serial connection through the DNP/5280 COM1 port or the 10/100 Mbps Ethernet interface for in-system programming.

3.6 10/100 Mbps Ethernet PHY

The DNP/5280 is using a Realtek RTL8201BL PHY 10/100Mbps chip that allows Ethernet connectivity with a speed up to 100Mbps. The RJ45 Ethernet interface on the Evaluation Board is just a simple connection over a transformer to the DIL interface pins, which are connected to the LAN controller onto the DNP/5280.

3.7 LAN Activity LEDs

These four miniature LEDs are placed on the DNP/5280 for a visual check of the LAN activity. Please refer to **chapter 4.5** for detailed information.

3.8 RTC DS1306

Real time clock circuit.

3.9 TTL

The 74AHC138 circuit is used for generating external chip selects.

3.10 TTL

The 74LVC541 circuit is used for the reset configuration of the Coldfire CPU.

3.11 J2 – 64-pin DIL Connector

The mechanical interface between the DNP/5280 and existing devices and equipment is a JEDEC 64-pin DIL connector with 2.54mm centers. This allows the direct integration to a standard 64-pin DIL socket.

Please refer to **chapter 4.2 and 4.3** for the complete pinout.

4 THE DNP/5280 IN DETAIL

4.1 Mechanical Dimensions

The DNP/5280 uses a 64-pin DIL socket as mechanical base. Figure 4-1 shows the dimensions. All length dimensions have a tolerance of 0.5 mm.

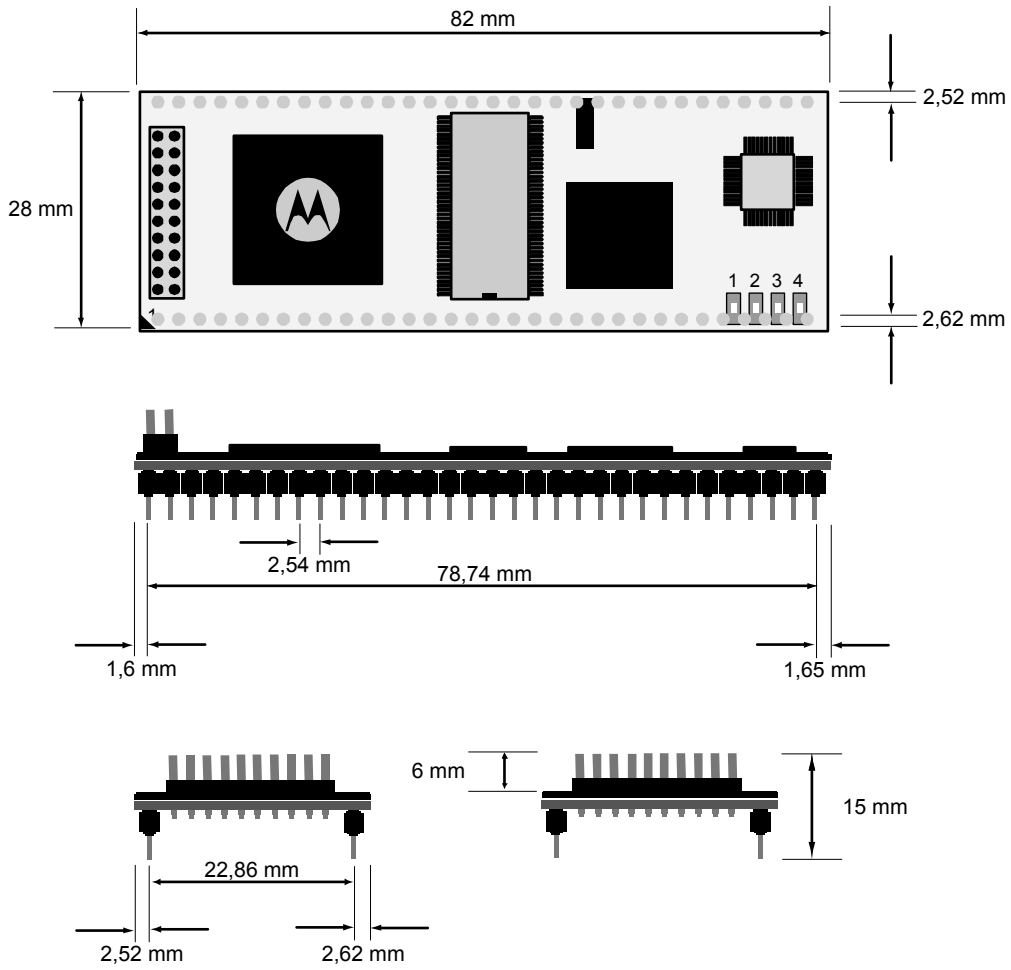


Figure 4-1: Mechanical dimensions of the DNP/5280

4.2 Pin Assignment – 64-pin DIL Connector (1. Part)

Pin	Name	Group	Function
1	PA0	PIO	Parallel I/O, Port A, Bit 0
2	PA1	PIO	Parallel I/O, Port A, Bit 1
3	PA2	PIO	Parallel I/O, Port A, Bit 2
4	PA3	PIO	Parallel I/O, Port A, Bit 3
5	PA4	PIO	Parallel I/O, Port A, Bit 4
6	PA5	PIO	Parallel I/O, Port A, Bit 5
7	PA6	PIO	Parallel I/O, Port A, Bit 6
8	PA7	PIO	Parallel I/O, Port A, Bit 7
9	PB0	PIO	Parallel I/O, Port B, Bit 0
10	PB1	PIO	Parallel I/O, Port B, Bit 1
11	PB2	PIO	Parallel I/O, Port B, Bit 2
12	PB3	PIO	Parallel I/O, Port B, Bit 3
13	PB4	PIO	Parallel I/O, Port B, Bit 4
14	PB5	PIO	Parallel I/O, Port B, Bit 5
15	PB6	PIO	Parallel I/O, Port B, Bit 6
16	PB7	PIO	Parallel I/O, Port B, Bit 7
17	PC0	PIO	Parallel I/O, Port C, Bit 0
18	PC1	PIO	Parallel I/O, Port C, Bit 1
19	PC2	PIO	Parallel I/O, Port C, Bit 2
20	PC3	PIO	Parallel I/O, Port C, Bit 3
21	RXD1	SIO	COM1 Serial Port, RXD Pin
22	TXD1	SIO	COM1 Serial Port, TXD Pin
23	CTS1	SIO	COM1 Serial Port, CTS Pin
24	RTS1	SIO	COM1 Serial Port, RTS Pin
25	DCD1	SIO	COM1 Serial Port, DCD Pin
26	DSR1	SIO	COM1 Serial Port, DSR Pin
27	DTR1	SIO	COM1 Serial Port, DTR Pin
28	RI1	SIO	COM1 Serial Port, RI Pin
29	RESIN	RESET	Reset Input
30	TX+	LAN	10/100 Mbps LAN, TX+ Pin
31	TX-	LAN	10/100 Mbps LAN, TX- Pin
32	GND	----	Ground

Table 4-1: DNP/5280 Pinout – Pin 1 to 32

4.3 Pin Assignment – 64-pin DIL Connector (2. Part)

Pin	Name	Group	Function
33	RX+	LAN	10/100 Mbps LAN, RX+ Pin
34	RX-	LAN	10/100 Mbps LAN, RX- Pin
35	RESOUT	RESET	Reset Output
36	VBAT	PSP	Real-Time Clock Battery
37	CLKOUT	PSP	Clock Output
38	TXD2	PSP	COM2 Serial Port, TXD Pin
39	RXD2	PSP	COM2 Serial Port, RXD Pin
40	INT5	PSP	Interrupt Input 5
41	INT4	PSP	Interrupt Input 4
42	INT3	PSP	Interrupt Input 3
43	INT2	PSP	Interrupt Input 2
44	INT1	PSP	Interrupt Input 1
45	CS4	PSP	Chip Select Output 4
46	CS3	PSP	Chip Select Output 3
47	CS2	PSP	Chip Select Output 2
48	CS1	PSP	Chip Select Output 1
49	IOCHRDY	PSP	I/O Channel Ready
50	IOR	PSP	I/O Read Signal
51	IOW	PSP	I/O Write Signal
52	SA3	PSP	Address Bit 3
53	SA2	PSP	Address Bit 2
54	SA1	PSP	Address Bit 1
55	SA0	PSP	Address Bit 0
56	SD7	PSP	Data Bit 7
57	SD6	PSP	Data Bit 6
58	SD5	PSP	Data Bit 5
59	SD4	PSP	Data Bit 4
60	SD3	PSP	Data Bit 3
61	SD2	PSP	Data Bit 2
62	SD1	PSP	Data Bit 1
63	SD0	PSP	Data Bit 0
64	Vcc	PSP	3.3 Volt Power Input

Table 4-2: DNP/5280 Pinout – Pin 33 to 64

4.4 DNP/5280 Function Multiplexing with 64-pin DIL Connector

Some pins of the 64-pin DIL connector of the DNP/5280 have multiple meanings. The pins have a primary and a secondary function (Function Multiplexing).
The primary functions correspond with the standard pinout of the 64-pin DIL connec-tor as shown in **table 4-1 and 4-2**. The secondary functions are shown in **table 4-3** below.

Pin	Name	Primary functions	Secondary functions
13	PB4	Parallel I/O, Port B, Bit 4	SCL (I2C)
14	PB5	Parallel I/O, Port B, Bit 5	SDA (I2C)
15	PB6	Parallel I/O, Port B, Bit 6	CANTX (CAN)
16	PB7	Parallel I/O, Port B, Bit 7	CANRX (CAN)
17	PC0	Parallel I/O, Port C, Bit 0	QSPIDO (SPI)
18	PC1	Parallel I/O, Port C, Bit 1	QSPIDI (SPI)
19	PC2	Parallel I/O, Port C, Bit 2	QSPICLK (SPI)
20	PC3	Parallel I/O, Port C, Bit 3	QSPICS0 (SPI)

Table 4-3: DNP/5280 Function Multiplexing

4.5 LAN Activity LEDs

Four miniature LEDs are placed on the DNP/5280 for a visual check of the LAN activity.

Name	Function	Description
LED 1	Link	Ethernet cable plugged in
LED 2	Duplex	Duplex-Mode
LED 3	10Act	Data transmission with 10 Mbps
LED 4	100Act	Data transmission with 100 Mbps

Table 4-4: DNP/5280 LEDs

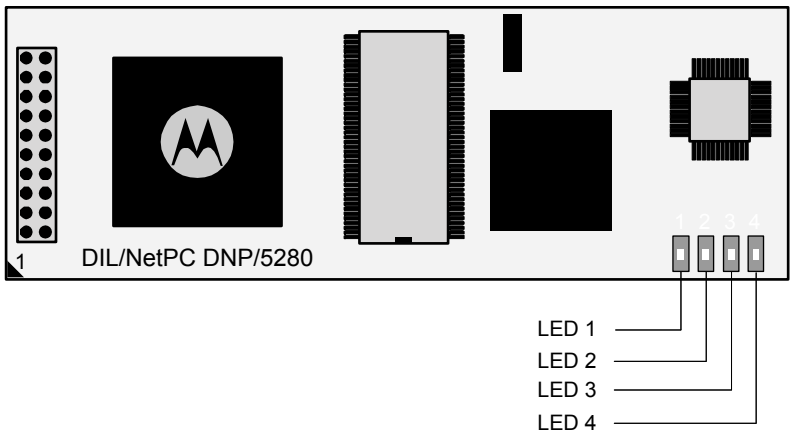
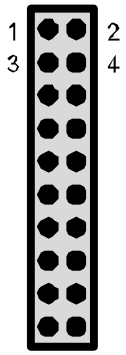


Figure 4-2: DNP/5280 LEDs

4.6 BDM-Interface



Pin	Name	Annotation
1	VIO (3.3 VDC I/O Voltage)	Power
2	GND	Ground
3	TA#	BDM-Function
4	BKPT#	BDM-Function
5	Reset#	BDM-Function
6	DSCLK#	BDM-Function
7	DSI#	BDM-Function
8	TCLK	BDM-Function
9	PST3	BDM-Function
10	DS0	BDM-Function
11	PST2	BDM-Function
12	DDATA3	BDM-Function
13	PST1	BDM-Function
14	DDATA2	BDM-Function
15	PST0	BDM-Function
16	DDATA1	BDM-Function
17	PSTCLK	BDM-Function
18	DDATA0	BDM-Function
19	GND	Ground
20	RCM	GPTB3

Table 4-5: DNP/5280 BDM-Interface

Pin 19 – Pin 20	Effects
Jumper not set	GPTB3 = 1 (High)
Jumper set	GPTB3 = 0 (Low)

Table 4-6: DNP/5280 RCM-Jumper

4.7 PIO-Mapping

The 20 Signals for the DNP/5280-Parallel-I/O (PIO) are realized through different function units of the MCF5280. The following table shows the assignment. Pin names for the MCF5280-case (256 MAPBGA) are listed in the third column. Please see the MCF5282 ColdFire Microcontroller User's Manual R.0.1 (MCF5282UM/D) for further details.

Pin	Name	MCF5280-Pinfunction	MCF5280-Pin
1	PA0	AN52	R4
2	PA1	AN53	T4
3	PA2	AN55	P3
4	PA3	AN56	R3
5	PA4	AN0	T3
6	PA5	AN1	R2
7	PA6	AN2	T2
8	PA7	AN3	R1
9	PB0	GPTA0	N13
10	PB1	GPTA1	P13
11	PB2	GPTA2	R13
12	PB3	GPTA3	T13
13	PB4	SCL	E15
14	PB5	SDA	E14
15	PB6	CANTX	E13
16	PB7	CANRX	D16
17	PC0	QSPIDO	F13
18	PC1	QSPIDI	E16
19	PC2	QSPICLK	F14
20	PC3	QSPICS0	F15

Table 4-7: DNP/5280 PIO-Mapping

4.8 DNP/5280 Expansion Bus Mapping

Pin	Name	Function	MCF5280 Signal	MCF5280 Pin	Remarks
40	INT5	Interrupt Input 5	IRQ7	B15	---
41	INT4	Interrupt Input 4	IRQ6	B16	---
42	INT3	Interrupt Input 3	IRQ5	C14	---
43	INT2	Interrupt Input 2	IRQ4	C15	---
44	INT1	Interrupt Input 1	IRQ3	C16	---
45	CS4	Chip Select Output 4	RAS1#	H13	See Device Errata
46	CS3	Chip Select Output 3	CS3#	L16	---
47	CS2	Chip Select Output 2	CS2#	L15	---
48	CS1	Chip Select Output 1	CS1#	L14	---
49	RDY	External Ready Input	TA#	P16	---
50	RD	Read Signal	OE#	N16	Also on-board use
51	WR	Write Signal	R/W#	N15	Also on-board use
52	SA3	Address Bit 3	A3	E3	Also on-board use
53	SA2	Address Bit 2	A2	E4	Also on-board use
54	SA1	Address Bit 1	A1	F1	Also on-board use
55	SA0	Address Bit 0	A0	F2	Also on-board use
56	SD7	Data Bit 7	D31	F3	Also on-board use
57	SD6	Data Bit 6	D30	G1	Also on-board use
58	SD5	Data Bit 5	D29	G2	Also on-board use
59	SD4	Data Bit 4	D28	G3	Also on-board use
60	SD3	Data Bit 3	D27	G4	Also on-board use
61	SD2	Data Bit 2	D26	H1	Also on-board use
62	SD1	Data Bit 1	D25	H2	Also on-board use
63	SD0	Data Bit 0	D24	H3	Also on-board use

Table 4-8: DNP/5280 Expansion Bus Mapping

4.9 DNP/5280 Memory Mapping

Function Unit	Startaddress	Endaddress	Access Format
SDRAM	0x0000.0000	0x00FF.FFFF	32 Bits
SRAM (intern)	0x2000.0000	0x2000.FFFF	32 Bits
CS1_Space	0x1000.0000	**0x100F**.FFFF	8 Bits
CS2_Space	0x1010.0000	0x101F.FFFF	8 Bits
CS3_Space	0x1020.0000	0x102F.FFFF	8 Bits
CS4_Space	0x1030.0000	0x103F.FFFF	8 Bits
IBSBAR	0x4000.0000	0x7FFF.FFFF	32 Bits
Flash (MCF5282 intern)	0xF000.0000	0xF007.FFFF	32 Bits
Flash	0xFF80.0000	0xFFFF.FFFF	16 Bits

Table 4-9: DNP/5280 Memory Mapping

The memory areas with names **CS1_Space** to **CS4_Space** are each assigned to the corresponding Chip Select Signals (CS1: Chip Select Output 1 to CS4: Chip Select Output 4) on the 64-pin DIL Connector.

In memory area **IBSBAR** the SFRs (Special Function Register) of the Motorola ColdFire MCF5280-Microcontroller are addressable.

User programs can only be loaded from 0x0001:0000 into the memory.

The DNP/5280 comes with a ROM-Monitor ex works. This ROM-Monitor needs a memory area in Flash and SDRAM each.

Function Unit	Startaddress	Endaddress
dBUG ROM-Monitor Code-Area	0xFF80.0000	0xFF83.FFFF
dBUG ROM-Monitor Data-Area	0x0000.0000	0x0000.FFFF

Table 4-10: DNP/5280 Reserved Areas for the ROM-Monitor

4.10 Connecting an External Battery

To ensure the RTC (Real Time Clock) function of the DNP/5280 when the main power is removed a backup battery must be connected between VBAT (pin 36) and GND. This backup battery should be a lithium battery with a voltage of approx. 3V DC. If main power is turned on – no battery power will be consumed.

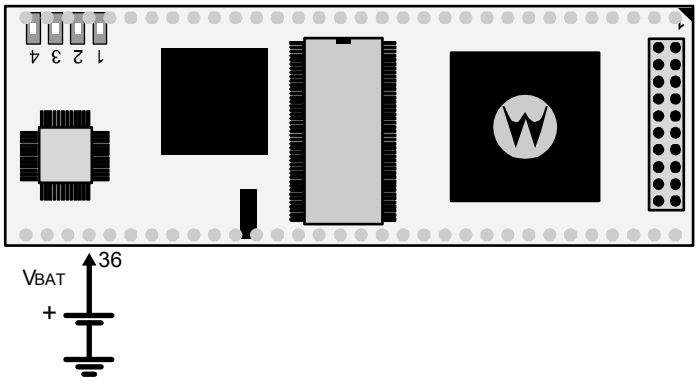


Figure 4-3: Connecting an external battery to pin 36 of the DNP/5280

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Revision	Date	Remarks	Name
1.0	2004-08-30	first version	WBU

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